WHAT IS CLAIMED IS:

1. A video signal processor comprising:

a memory that utilizes a first clock signal for writing a video data signal and a second clock signal for reading a video data signal;

a delay unit, including plural delay elements, for delaying the second clock signal;

a selector for selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed using the respective delay elements of the delay unit, and outputs phase information of the selected clock;

an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and

an interpolator for interpolating the video data signal read from the memory in accordance with the second clock signal using the interpolation factor.

2. A video signal processor comprising:

a memory that utilizes a first clock signal for writing a video data signal and a second clock signal for reading a video data signal;

a delay unit, including plural delay elements that can vary respective delay elements, for delaying the second clock signal by one period of the second clock signal;

a phase comparator for comparing phases between a clock that is obtained by delaying a focus clock in the second clock signal by one clock using the delay unit, and a clock that is one clock later than the focus clock;

a controller for controlling respective delay values of the delay elements of the delay unit on the basis of a phase difference detected by the phase comparator;

a selector for selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed by the respective delay elements of the delay unit, and outputting phase information of the selected clock;

an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and

an interpolator for interpolating the video data signal read from the memory in accordance with the second clock signal using the interpolation factor.

3. A video signal processor comprising:

a memory that utilizes a first clock signal for writing or reading a video data signal;

a delay unit, including plural delay elements, for delaying the first clock signal;

a selector for selecting a clock that is most synchronized

with a reference signal inputted from outside, from among clocks that have been delayed using the respective delay elements of the delay unit, and outputting phase information of the selected clock;

an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and

an interpolator for interpolating the video data signal read from the memory in accordance with the first clock signal using the interpolation factor.

4. A video signal processor comprising:

a memory that utilizes a first clock signal for writing or reading a video data signal;

a delay unit, including plural delay elements that can vary respective delay values, for delaying the first clock signal by one period of the first clock signal;

a phase comparator for comparing phases between a clock that is obtained by delaying a focus clock in the first clock signal by one clock using the delay unit, and a clock that is one clock later than the focus clock;

a controller for controlling the respective delay values of the delay elements of the delay unit on the basis of a phase difference detected by the phase comparator;

a selector for selecting a clock that is most synchronized

with a reference signal inputted from outside, from among clocks that have been delayed by the delay elements of the delay unit, and outputting phase information of the selected clock;

an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and

an interpolator for interpolation the video data signal read from the memory in accordance with the first clock signal using the interpolation factor.

5. A video signal processing method including the steps of:

writing a video data signal into a memory in accordance with a first clock signal;

delaying a second clock signal using plural delay elements;

selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed by the delay elements, and generating phase information of the selected clock;

converting the phase information into an interpolation factor; and

interpolating the video data signal read from the memory in accordance with the second clock signal using the interpolation factor.